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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/775,966	**Applicant(s)** PRITCHARD ET AL.
	Examiner Vuthe Siek	**Art Unit** 2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 April 2007.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/775,996 filed on 4/23/2007. Claims 1-27 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Oh (6,996,016 B2).

4. As to claims 1, 11 and 21, Oh teaches a method and a circuit configuration for implementing a double data rate feature in a memory device capable of operating in a variable latency mode (read as a method and a configuration circuit for configuring on a programmable chip) (see col. 2 lines 40-67; col. 3 lines 1-3). The implementation of the circuit configuration includes placing and establishing connections between a primary component and second component as shown in Fig. 1. The establishment of connections includes establishing a plurality of transmission lines (Fig. 1, unidirectional and bi-directional of system bus 106 and 114 and data bus line 108; col. 4 lines 1-50). The method for implementing the circuit configuration that is operating on both fixed latency and variable latency (col. 2 lines 45-67; col. 3 lines 1-3). In order to establishing

connections at least the methods that provide this circuit configuration must receiving information associated with a primary component (at least knowing a primary component that is a processor as shown in Fig. 1) and information associated with a secondary component (at least knowing a secondary component that is memory as shown in Fig. 1), the primary component having either fixed latency or variable latency characteristics. Fig. 1 shows burst PSRAM devices that are operating in both fixed and variable latency mode in response to requests from the primary component (col. 2 lines 45-57; col. 4 lines 1-50). As described earlier, in order to implementing a circuit configuration (meaning placing and establishing connections between the primary component and secondary component as shown in Fig. 1, the implementation of the circuit configuration must generating an interconnection module coupling the primary component to the secondary component, where the interconnection module including data, address and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components (Fig. 1 shown a plurality of transmission lines that are formed a interconnection module as claims). A plurality of transmission lines is used for establishing connections between the primary component and second component as shown in Fig. 1 (col. 4 lines 1-50). In order to establishing connections between the primary component and secondary component as shown in Fig. 1, the methods for implementing the circuit configuration as in Fig. 1 must including a selection mechanism to a user to have the primary component (processor or system controller as shown in Fig. 1) access the secondary component (burst PSRAM devices as shown as memory in Fig. 1) using fixed latency or variable latency (col. 2 lines 45-67;

col. 3 lines 1-3), wherein the input interface (computer for implementing the circuit configuration as shown in Fig. 1) receiving the selection from the user to have the primary component issue a plurality of reads to the secondary component using variable latency in response to providing the selection mechanism (Col. 4 lines 1-50). Figs. 3-7 show timing diagrams.

5. As to claims 2, 12 and 22, Oh teaches the limitations of interconnection module including data, address, and control lines including a data valid line indicating that data is available for transfer from the secondary component (at least see col. 4, lines 1-50; Fig. 1).

6. As to claims 3, 13 and 23, Oh teaches the secondary component is operable to receive multiple requests from the primary component before responding (at least see Fig. 1, col. 4, lines 15-50; Figs. 3-7 show timing diagrams).

7. As to claims 4, 14 and 24, Oh teaches the secondary component asserts a wait request line if the secondary component can no longer receive any additional requests (at least see Fig. 1, col. 4, lines 15-50; Figs. 3-7 show timing diagrams).

8. As to claims 5, 15 and 25, Oh teaches the data valid line allows a secondary component read transfer with variable latency (Read cycle of a variable latency mode; at least see Fig. 1; col. 3 lines 62-67).

9. As to claims 6, 16 and 26, Figs. 3-7 show timing diagrams of signals which might appear on corresponding transmission lines of the system and data buses of DDR Burst PSRAM device in Read cycle of a variable latency mode (Fig. 3); in Write cycle of a fixed latency mode (Fig. 4); in Write cycle of a variable mode (Fig. 5); in Write cycle of a

variable mode (Fig. 6); in Write cycle of a variable mode (Fig. 7). These variable latency modes are configured by designer (user) while selecting the primary and secondary components. Fig. 2 example of a multiple secondary components. Note that Oh teaches many integrated circuits are benefited from his invention.

10. As to claims 7, 17 and 27, Oh teaches a method of operating a double data rate burst PSRAM memory device in a variable latency mode in Read cycle and a fixed latency mode in Write cycle latency mode or in the variable latency mode in both Read and Write cycles. The method uses a WAIT_DQS signal that combines functions of a data strobe (DQS) signal and a WAIT signal that indicates to a system controller of the DDR burst PSRAM memory device when valid data is present on a data bus in Read cycle and when memory is ready to accept data in Write cycle. The WAIT_DQS signal is initiated by the memory in Read cycle of a variable latency mode by the system controller in Write cycle of a fixed latency mode. In Write cycle of a variable latency mode, the memory and system controller sequentially initiate the WAIT_DQS signal (summary). Figs. 3-7 show and describe timing diagrams of the system controller and memories operable in both fixed and variable latency modes via interconnection module. Fig. 2 shows the interconnection module comprising a simultaneous multiple memory fabric, where the system controller able to simultaneously access component memories. Oh teaches that his invention benefits many applications of integrated circuits. These teachings suggest that interconnection module also must comprise a simultaneous multiple primary component fabric so that multiple primary components

are capable to access the secondary component simultaneously (e.g. memory) when needed.

11. As to claims 8 and 18, Oh teaches that the secondary component (Burst PSRAM device) initiates WAIT_DQS signal that is a combined function of WAIT and DQS (Figs. 3-7). These suggest that the burst PSRAM is associated with a buffer for holding data available for transfer form the secondary component (burst PSRAM device).

12. As to claims 9 and 19, Oh teaches the primary component is a system controller (a generic processor module from a component library) (Fig. 1, col. 4 lines 1-14).

13. As to claims 10 and 20, Oh teaches the secondary component is a burst PSRAM (a generic memory module from a component library) (Figs. 1-2; col. 4 lines 1-14; col. 7 lines 16-20).

14. Claims 1-7, 11-17 and 21-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Wingard et al. (6,725,313 B1).

15. As to claims 1, 11 and 21, Wingard et al. teach substantially the same claim limitations comprising a primary component having either fixed latency or variable latency characteristics; a secondary component having either fixed latency or variable latency characteristics, wherein the secondary component is operable to respond to requests from the primary component; and an interconnection module coupling the primary component to the secondary component, wherein the interconnection module supports a system having both fixed latency and variable latency characteristics (Figs. 1, 5 or 11; Fig. 11 shows master (primary component); slave (secondary component) and interconnection module 1010 for interconnecting there between the master and

salve; Fig. 5 shows the same having plurality of masters (primary components), slaves (secondary components) and interconnection module for interconnecting there between the primary components and secondary components). The system supports both fixed latency and variable latency characteristics (at least see col. 6 lines 59-67; col. 7 lines 1-67; col. 8 lines 1-11). In order to establishing connections between the primary component and secondary component, a selection mechanism as recited must be included.

16. As to claims 2, 12 and 22, Wingard et al. teach data, address, control lines including a data valid line (at least see col. 7 lines 25-67).

17. As to claims 3, 13 and 23, Wingard et al. teach the secondary component receiving multiple requests from the primary component before responding (at least see Fig. 11; Figs. 6-10 show timing diagrams of requests and responses).

18. As to claims 4, 14 and 24, Wingard et al. teach asserted (col. 13 lines 55-67).

19. As to claims 5, 15 and 25, Wingard et al. teach data valid line allows a secondary component read transfer with variable latency (col. 7 lines 1-67; col. 8 lines 1-11).

20. As to claims 6, 16 and 16, Wingard et al. teach a system having primary components, secondary components and interconnection module for interconnecting there between that supports fixed latency and variable latency characteristics. This clearly suggests that designer or user must configure variable latency while selecting the primary and secondary latency in order to provide proper interconnection between selected primary component and selected secondary components.

21. As to claims 7, 17 and 27, Wingard et al. teach interconnection module comprising a simultaneous multiple primary component fabric (Fig. 5). Fig. 5 shows interconnection module that two components (primary) can simultaneously access to other component.

Remarks

22. Applicant argued that Oh is not believed to teach or suggest receiving information about the primary component and second component and generating an interconnection module coupling the primary component to the secondary component, the interconnection module include data, address and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency. Examiner disagrees. Oh teaches methods for implementing a circuit configuration comprising a primary component and secondary component. The implementation of the circuit configuration includes establishing connections between the primary component and second component, where circuit configuration is operating in both fixed latency and variable latency mode (see summary, col. 3 lines 63-67; col. 4 lines 1-50). The establishment of connections as described earlier and shown in Fig. 1 form an interconnection module as claimed. The interconnection module as shown in Fig. 1 (a plurality of transmission lines described in col. 4 lines 1-50) includes data, address and control lines (buses 108 and 114 including data, address and control lines, col. 4 lines 1-50). The synthesized circuit configuration as in Fig. 1, comprising establishing connections of transmission lines (known as interconnection module as recited in the claims), the circuit configuration as in Fig. 1 supports a system having

fixed and variable latency components (col. 1 lines 5-10; lines 35-39; col. 2 lines 40-44; summary). Examiner believes that receiving information associated with the first component (processor) and second component (memory) is inherent in the art. In order to obtain or generate or synthesized an IC architecture as shown in Fig. 1, the information associated with the processor (primary component) and memory (second component) must be known and received. The interconnection module (system controller and buses) is coupled between the processor and memory to support fixed and variable latency components. Clearly Oh teach the invention generally provides method and circuit configuration for implementing a double data rate feature in memory device capable of operating in a variable latency mode in Read and/or Write cycles, such as burst PSRAM devices (col. 3 lines 62-67). Thus limitation of a processor configured to generate interconnection module as described above is inherently in the art. Fig. 1 clearly shown a generated interconnection module (system controller and buses 114 and 108) is coupled between the processor (primary component) and memory (second component). Therefore, Examiner believes that the claim invention as recited is anticipated by Oh. In addition, Applicant did not respond to Wingard et al. (6,725,301) teachings. It appears to believe that Applicant agrees that Wingard et al. teach the claim invention as in above rejection. Examiner respectively submits that the claimed limitations as anticipated by the teachings of the references. Claims do not specifically recited what information associated related to a primary component and secondary component. The interconnection module generated is recited in the claims. The references teach implementing a circuit configuration that including establishing

connections between the primary component and secondary component. This is read as an interconnection module generated as recited in the claims. Applicants argued that the references taught standard bus. Examiner disagreed. Based on the claim language the interconnection module generated could be standard bus. The interconnection module is interpreted as connections that are formed to establishing connections between the primary component and the secondary component. In order to establishing the connections, a selection mechanism as recited must be included. Clearly as shown in Fig. 1 of Ono, in the implementation of the circuit configuration as shown in Fig. 1 to support both fixed latency and variable latency, transmission lines are used to establish connections between the primary component and secondary component. These transmission lines are formed an interconnection module as recited in the claims. Examiner does not see the difference based on the claim language.

23. This is a continuation of applicant's earlier Application No. 10/775,966. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, A.U. 2825